

# NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL

DEPARTMENT OF CENTRE FOR SYSTYEM DESIGN, NITK SURATHKAL

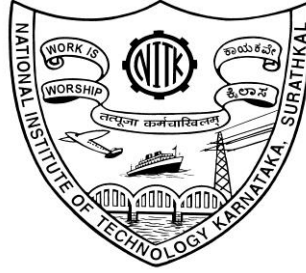
POST SRINIVASNAGAR, MANGALORE – 575 025 (D K)

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## TENDER DOCUMENT

Tender Notification No: NITK/CSD/DHI-BLDC/2020/APCDS/YK-04

Date:20/08/2020

Name of Goods	: Altium PCB Design Software
Estimated amount put to Tender	: ₹ 4,50,000/- (Including GST)
EMD Amount (2% of estimated amount)	: Rs. 9,000/-
Time for Supply of item	: 04 Weeks
Date for Request tender document	: 11/09/2020, 03.00 p.m.
End date for submission of e-tender	: 11/09/2020, 04.00 p.m.
Address for Submission of Tender	: <a href="https://mhrd.euniwizarde.com">https://mhrd.euniwizarde.com</a>
Opening date of technical bid	: 14/09/2020, 04.00 pm
Contact Details of Buyer	: <b>Dr. Yashwant Kashyap</b> Asst. Professor, Dept. of Electrical & Electronic Engineering, NITK Surathkal – 575025 Ph: 0824-24743915, <a href="mailto:yashwant.kashyap@nitk.edu.in">yashwant.kashyap@nitk.edu.in</a>



# NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL

POST SRINIVASNAGAR, MANGALURU – 575 025

(An Autonomous Body of the Ministry of HRD, Govt. of India)

Phone: (0824) 2474 000.  
Email: registrar@nitk.ac.in

Fax: (0824) 2474 033/ 2474 039  
Website: <http://www.nitk.ac.in>

**Tender Notification No: NITK/CSD/DHI-BLDC/2020/APCDS/YK-04**

**Date:20/08/2020**

## **NOTICE INVITING e-TENDER (e-NIT)**

The National Institute of Technology Karnataka, Surathkal (in short – NITK, Surathkal) is an autonomous institute under Ministry of HRD Govt of India imparting Technical Education and engaged in Research Activities. It is proposed to procure equipment for Central Research Facility.

Online Tender (<https://mhrd.euniwizarde.com/>) is invited for the following items in **two cover system** (i.e., Technical bid and financial bid) subject to the following terms and conditions, from the reputed manufacturers or it's authorized dealers so as to reach this office on or before scheduled date and time. The tender (Technical bid) will be opened online on the due date as mentioned. Bidders can verify their bid status through online portal <https://mhrd.euniwizarde.com/>. The financial bid of only such bidders whose technical bid is accepted shall be opened on the same day or later pre-informed date.

- |  |   |
|--|---|
| 1. Name of Goods                       | : Altium PCB Design Software  |
| 2. Estimated Cost                      | : ₹ 4,50,000/- (Including GST)  |
| 3. E M D (2% of estimated amount)      | : Rs 9,000/-  |
| 4. Date for Request tender document    | : 11/09/2020, 03.00 p.m.  |
| 5. End date for submission of e-tender | : 11/09/2020, 04.00 p.m.  |
| 6. Address for Submission of Tender    | : <a href="https://mhrd.euniwizarde.com">https://mhrd.euniwizarde.com</a>   |
| 7. Date of opening of technical bid    | : 14/09/2020, 04.00 p.m.  |
| 8. Contact Details of Buyer            | : Dr. Yashwant Kashyap<br>Asst. Professor,<br>Dept. of Electrical & Electronic Engineering,<br>NITK Surathkal – 575025<br>Ph: 0824-24743915, yashwant.kashyap@nitk.edu.in |

**Sd/-  
Co-ordinator**

## **SECTION 1 A:- PROCEDURE FOR SUBMISSION OF E-TENDER**

The bidders are required to submit soft copies of their bid electronically on the e-Wizard Portal using valid Digital Signature Certificates. Below mentioned instructions are meant to guide the bidders for registration on the e-Wizard Portal, prepare their bids in accordance with the requirements and submit their bids online on the e-Wizard Portal. For more information bidders may visit the e-Wizard Portal <https://mhrd.euniwizarde.com>

### **1. REGISTRATION PROCESS ON ONLINE PORTAL**

1. Bidders to enroll on the e-Procurement module of the portal <https://mhrd.euniwizarde.com> by clicking on the link "Bidder Enrolment" as per portal norms.
2. The bidders to choose a unique username and assign a password for their accounts. Bidders are advised to register their valid email address and mobile numbers as part of the registration process. These would be used for any communication from the e-Wizard Portal.
3. Bidders to register upon enrolment their valid Digital Signature Certificate (DSC: Class II or Class III Certificates with signing key usage) issued by any Certifying Authority recognized by CCA India with their profile.
4. Only one valid DSC should be registered by a bidder. Please note that the bidders are responsible to ensure that they do not lend their DSCs to others which may lead to misuse. Foreign bidders are advised to refer "DSC details for Foreign Bidders" for Digital Signature requirements on the portal.
5. Bidder then logs in to the site through the secured log-in by entering their user ID/password and the password of the DSC / e-Token.

### **2. TENDER DOCUMENTS SEARCH**

1. Various built-in options are available in the e-Wizard Portal which is further synchronizing with CPP Portal to facilitate bidders to search active tenders by several parameters. These parameters include Tender ID, organization, location, date, value, etc.
2. There is also an option of advanced search for tenders, wherein the bidders may combine a number of search parameters such as organization name, a form of contract, location, date, other keywords, etc. to search for a tender published on the Online Portal.
3. Once the bidders have selected the tenders they are interested in, they may download the required documents/tender schedules. These tenders can be moved to the respective 'My Tenders' folder. This would

enable the Online Portal to intimate the bidders through SMS / e-mail in case there is any corrigendum issued to the tender document.

4. The bidder should make a note of the unique Tender ID assigned to each tender, in case they want to obtain any clarification/help from the Helpdesk.

### **3. BID PREPARATION**

1. Bidder should take into account any corrigendum published on the tender document before submitting their bids.
2. Please go through the tender advertisement and the tender document carefully to understand the documents required to be submitted as part of the bid.
3. Please note the number of covers in which the bid documents have to be submitted, the number of documents - including the names and content of each of the document that needs to be submitted. Any deviations from these may lead to rejection of the bid.
4. Bidder, in advance, should get ready the bid documents to be submitted as indicated in the tender document/schedule and generally, they can be in PDF / XLS / PNG, etc. formats. Bid documents may be scanned with 100 dpi with black and white option.

### **4. BID SUBMISSION**

1. Bidder to log into the site well in advance for bid submission so that he/she uploads the bid in time i.e. on or before the bid submission time. Bidder will be responsible for any delay due to other issues.
2. The bidder to digitally sign and upload the required bid documents one by one as indicated in the tender document.
3. Bidder to select the payment option as "Online" to pay the tender fee/ EMD wherever applicable and enter details of the instrument.
4. A standard BoQ format has been provided with the tender document to be filled by all the bidders. Bidders to note that they should necessarily submit their financial bids in the prescribed format and no other format is acceptable.
5. The server time (which is displayed on the bidders' dashboard) will be considered as the standard time for referencing the deadlines for submission of the bids by the bidders, the opening of bids, etc. The bidders should follow this time during bid submission.

6. All the documents being submitted by the bidders would be encrypted using PKI encryption techniques to ensure the secrecy of the data, which cannot be viewed by unauthorized persons until the time of bid opening.
7. The uploaded tender documents become readable only after the tender opening by the authorized bid openers.
8. Upon the successful and timely submission of bids, the portal will give a successful bid submission message & a bid summary will be displayed with the bid no. and the date & time of submission of the bid with all other relevant details.
9. Kindly have all relevant documents in a single PDF file of compliance sheet.
10. **The off-line tender shall not be accepted and no request in this regard will be entertained whatsoever.**

## **5. AMENDMENT OF BID DOCUMENT**

At any time prior to the deadline for submission of proposals, the institutions reserve the right to add/modify/delete any portion of this document by the issuance of a Corrigendum, which would be published on the website and will also be made available to the all the Bidder who has been issued the tender document. The Corrigendum shall be binding on all bidders and will form part of the bid documents.

## **6. ASSISTANCE TO BIDDERS**

1. Any queries relating to the tender document and the terms and conditions contained therein should be addressed to the Tender Inviting Authority for a tender or the relevant contact person indicated in the tender.
2. Any queries relating to the process of online bid submission or queries relating to e-Wizard Portal, in general, may be directed to the 24x7 e-Wizard Helpdesk. The contact number for the helpdesk is **011-49606060, 23710092, 23710091, Sanjeet Kumar Jha +91-8882495599, 9350530626, Gagan +91 8448288987, 8448288988 and Vijay +91 9113518121, 8448288989**

## **7. INSTRUCTIONS TO THE BIDDERS**

1. **Process for Bid submission through MHRD portal is explained in Bidder Manual. Bidders are requested to download Bidder Manual from the home page of MHRD website (<https://mhrd.euniwizarde.com>). Steps are as follows (Home page  $\Rightarrow$  Downloads  $\Rightarrow$  Bidder Manuals).**
2. The tenders will be received online through portal <https://mhrd.euniwizarde.com>. In the Technical Bids, the bidders are required to upload all the documents in .pdf format.

3. Possession of Valid Class II/III Digital Signature Certificate (DSC) in the form of smart card/ e-Token in the company's name is a prerequisite for registration and participating in the bid submission activities through <https://mhrd.euniwizarde.com>. Digital Signature Certificates can be obtained from the authorized certifying agencies, details of which are available on the web site <https://mhrd.euniwizarde.com> under the link 'DSC help'.

Tenderers are advised to follow the instructions provided in the 'Instructions to the Tenderers for the e-Submission of the bids online through the e-Wizard Portal for e-Procurement at <https://mhrd.euniwizarde.com>.

4. **The bidder has to "Request the tender" to MHRD portal before the "Date for Request tender document", to participate in bid submission.**
8. All entries in the tender should be entered in online Technical & Commercial Formats without any ambiguity.
9. Any order resulting from this e-tender shall be governed by the terms and conditions mentioned therein.
10. No deviation to the technical and commercial terms & conditions are allowed.
11. The tender inviting authority has the right to cancel this e-tender or extend the due date of receipt of the bid(s).

## SECTION 1 B: INSTRUCTION TO BIDDER (ITB)

1. **The bid should be submitted in two covers System-Technical Bid and Financial Bid** online through portal <https://mhrd.euniwizarde.com>:

1.1 **Envelope No.1 – Technical Bid:** The agencies should give details of their technical soundness and provide a list of customers of a previous supply of similar items to Universities, Institutes or Government Departments/ Undertakings/ public sectors with contact details. The details of the Bidder/ profile should be furnished along with the copy of all related documents. This envelope should be uploaded **online tender (<https://mhrd.euniwizarde.com/> )** and digitally signed as **“Envelope No. 1 – Technical Bid i.e. Checklist (Excel format).**

1.2. **Document to be scanned and submitted by uploading in the technical bid:**

- a) The Bidder should possess a Licence certificate for manufacture /supply of the item.
- b) List of Owner/partners of the firm and their contact numbers
- c) The Bidder should possess Income-tax PAN Number.
- d) The Bidder should possess a valid GST registration number.
- e) Catalogue of the Product with detailed product specifications.
- f) List of Service Centres
- g) List of customers with contact details.
- h) The average annual turnover should not be less than 30% of the estimated cost put to tender/Tender for the job work. The copy of the Balance sheet, Profit & Loss A/c., Trade or Manufacturing A/c for the last 3 years should be enclosed
- i) **Warranty Period Offered for the tendered item to be specified. If the Warranty period is not conforming to the schedule of requirements given in section 3 of the document, the bid is liable to be treated as non-responsive and rejected.**
- j) **EMD payment needs to make through Online. EMD shall bear no interest. Any bid not accompanying with EMD is liable to be treated as non-responsive and rejected.**
- k) NSIC/ MSME registration certificate (in case of bidders claiming exception of EMD while submitting a bid)
- l) **Contract form given in section 5 needs to be submitted.**

**The above documents should be furnished in the technical bid envelope.**

2. Envelope No.2 – Financial bid: The agencies should submit their financial bid as per the (.xlsx) format is given in Section 4 of the Notice Inviting Tender in this cover. The rate should be quoted in figures and upload online bid.This envelope should upload online only as “Envelope No. 2 – Financial Bid”.

Both the Envelope No. 1 and 2 should be uploaded through online portal (<https://mhrd.euniwizarde.com>).

- 3 The tender will be accepted only from the **manufacturers or its authorised supplier**.
4. The Institute **reserves the right to visit the factory** before or after the issue of supply order to satisfy itself regarding the quality of production. In case of any remarks /default noted, the EMD will be forfeited even if pre-qualified.
5. **The Financial Bid shall be in the format of Price Schedule given in Section 4. The Contract form as per format is given in section 5 shall be submitted. The incomplete or conditional tender will be rejected.**
6. Details of the item to be carried out, approximate quantity and the specifications are mentioned in **“Section 3”** appended to this Notice Inviting Tender.
7. **The item to be used is strictly according to the specification and subject to test by the Institute/concerned authorities. It must be delivered and installed in good working condition.**
8. The Institute **reserves the right to cancel or reduce the quantity** included in the schedule of requirements at any time after acceptance of the tender with a notice. The Contractor/Supplier shall have no claim to any payment of compensation or otherwise whatsoever, on account of any profit or advantage which he might have derived from the execution of the work/supply in full but he did not derive in consequence of the foreclosure of the whole or part of the works.
9. **Performance Security of 5 % of the contract value in terms of Bank Guarantee by scheduled banks shall be given by the successful bidder for the total period of Warranty.**
10. **The release of EMD:** The EMD shall be released after receipt of performance security from the successful bidder.
- 11 **The validity of bids:** The rate quoted should be valid for a minimum of 90 days. No claim for escalation of the rate will be considered after opening the Tender.
- 12 **Clarification of Tender Document:**  
A prospective bidder requiring any clarification of the Tender Document may communicate to the contact person given in this notice inviting tender. The contact person will respond to any request for clarification for the Tender Document received not later than 5 working days prior to the last date for the receipt of bids
- 13 **Amendment of Tender document:** At any time prior to the last date for receipt of bids, Institute may for any reason, whether at its own initiative or in response to a clarification requested by a prospective bidder, modify the Tender document by an amendment.
- 14 **Institute may at its own discretion extend the last date for the receipt of bids.**
- 15 The bids shall be written in English language and any information printed in another language shall be accompanied by an English translation, in which case for the purpose of interpretation of the bid, the English translation shall govern.



- 16 The Institute reserves the right of accepting any bid other than the lowest or even rejecting all the bids. The decision of the Institute Purchase Committee is final in all matters of tender and purchase.
- 17 The bidder should give the following declaration while submitting the Tender.
- 18 Relaxation for Start-up, MSEs, Make in India will be as per GOI norms.
- 19 Any other details required may be obtained from the contact person (Buyer) given in the Notice Inviting Tender during the office hours.

## DECLARATION

I/we have not tampered/modified the tender forms in any manner. In case, if the same is found to be tampered/modified, I /we understand that my/our tender will be summarily rejected and full Earnest money deposit will be forfeited and I /we are/are liable to be banned from doing business with NITK, Surathkal and/or prosecuted.

**Signature of the Bidder** : \_\_\_\_\_

**Name and Designation** : \_\_\_\_\_

**Business Address** : \_\_\_\_\_  
\_\_\_\_\_

**Place:**

**Seal of the Bidder's Firm**

**Date:**

## SECTION 2: CONDITIONS OF CONTRACT

1. The supplier should quote the rate for Door Delivery (FOR).
2. The Rate should be quoted in INR only.
3. No custom duty exemption certificate will be provided from the institute.
4. NITK is a DSIR recognized research organization and hence eligible for concessional / exempted rate of GST @5% (For indigenous items).
5. The rate quoted should be on a unit basis. Taxes and other charges should be quoted separately, duly considering exemptions if any.
6. Rate quoted should be inclusive of Testing, commissioning and installation of equipment and Training.
7. Payment: No advance payment will be made. Payment will be made only after the supply of the item in good and satisfactory condition and receipt of performance security by the supplier.
8. Guarantee and Warranty period should be specified for the complete period conforming to section 3 of this tender document.
9. The period required for the supply and installation of the item should be specified conforming to section 3 of this tender document.
10. In case of dispute, the matter will be subject to Mangalore Jurisdiction only.

### SECTION 3: SCHEDULE OF REQUIREMENTS, SPECIFICATIONS AND ALLIED DETAILS

[To be filled up by the Department / Center of NITK, Surathkal]

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Item(s) Name to be procured : Altium PCB Design Software

Type (Equipment / Software / Furniture / Others) : Software

Brief Specifications of the Item(s) : **As per Annexure "A"**  
(Attach Additional Sheet if necessary)

Quantity : 1 No

Any other details / requirement : Nil

Warranty Period required : 01 Year

Delivery Schedule expected  
after release of Purchase order  
(In Weeks) : 04 Weeks

EMD (in Rupees) : Rs. 9,000/-

Performance Security to be given  
by Successful Bidder after release of  
Purchase Order (in Rupees) : 5% of PO value

**SECTION 4 - PRICE BID**  
**[To be used by the bidder for submission of the bid]**

Reference Number:

Date:

Sr. No.	Description of the Item and Specification	Qty. in Units	Unit Price (Rs.)	Discount %	GST (%)	Other charges if any (please specify details)	Total Price (Rs.)
1							
2							

1. Delivery Mode: Delivery at NITK Surathkal, at the site only.

Total Bid Price in the above column should be inclusive of all taxes and levies transport, loading, unloading, etc.

Delivery Period:..... days.

Validity Date: Minimum 90 days from the date of submission of Tender/Tender.

2. Payment Term: Payment within 30 days from the date submission of bill Acceptance Certificate to concerned Dept./ Sect.

PAN No. : .....

GST Registration No. : .....

Seal and Signature:.....

Name & Business Address:.....

**Note: Price Bid should be submitted in given format only.**

Place:

Date:

**SECTION 5: CONTRACT FORM**

[To be provided by the bidder in the business letter head]

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1. (Name of the Supplier's Firm) hereby abide to deliver them by the delivery schedule mentioned in section 3 tender document for the supply of the items if the purchase order is awarded.
2. The item will be supplied conforming to the specifications stated in the tender document without any defect and deviations.
3. Warranty will be given for the period mentioned in the tender document and service will be rendered to the satisfaction of NITK, Surathkal during this period.

**Signature of the Bidder** : \_\_\_\_\_

**Name and Designation** : \_\_\_\_\_

**Business Address** : \_\_\_\_\_

\_\_\_\_\_

**Place:**

**Seal of the Bidder's Firm**

**Date:**

## BANK GUARANTEE FORMAT FOR PERFORMANCE GUARANTEE BOND

(To be typed on Non-judicial stamp paper of the value of Indian Rupees of One Hundred) (TO BE ESTABLISHED THROUGH ANY OF THE NATIONAL BANKS (WHETHER SITUATED AT MANGALORE OR OUTSTATION) WITH A CLAUSE TO ENFORCE THE SAME ON THEIR LOCAL BRANCH AT MANGALORE OR ANY SCHEDULED BANK (OTHER THAN NATIONALISED BANK) SITUATED AT MANGALORE. BONDS ISSUED BY CO-OPERATIVE BANKS ARE NOT ACCEPTED.)

To,  
Registrar,  
National Institute of Technology Karnataka,  
Srinivasnagar P.O., Surathkal  
Mangalore – 575025

### LETTER OF GUARANTEE

WHEREAS National Institute of Technology Karnataka (Buyer) has invited Tenders vide Tender No..... Dt. .... for purchase of ..... AND WHEREAS the said tender document requires that any eligible successful tenderer (seller) wishing to supply the equipment / machinery, etc. in response thereto shall establish an irrevocable Performance Guarantee Bond in favour of “**Registrar, National Institute of Technology Karnataka, Surathkal**” in the form of Bank Guarantee for Rs ..... (**10% (ten percent) of the purchase value**) and valid till **one year or up to warranty period whichever is later** from the date of issue of Performance Guarantee Bond may be submitted within 30 (Thirty) days from the date of Order Acknowledgement as a successful bidder.

NOW THIS BANK HEREBY GUARANTEES that in the event of the said tenderer (seller) failing to abide by any of the conditions referred in tender document / purchase order / performance of the equipment / machinery, etc. this Bank shall pay to National Institute of Technology Karnataka, Surathkal on demand and without protest or demur Rs ..... (Rupees.....).

This Bank further agrees that the decision of National Institute of Technology Karnataka, Surathkal (Buyer) as to whether the said Tenderer (Seller) has committed a breach of any of the conditions referred in the tender document/purchase order shall be final and binding.

We, ..... (name of the Bank & branch) hereby further agree that the Guarantee herein contained shall not be affected by any change in the constitution of the Tenderer (Seller) and/ or National Institute of Technology Karnataka, Surathkal (Buyer).

#### Notwithstanding anything contained herein:

1. Our liability under this Bank Guarantee shall not exceed Rs. .... (Indian Rupees ..... only).
2. This Bank Guarantee shall be valid up to .....(date) and
3. We are liable to pay the guaranteed amount or any part thereof under this bank guarantee only and only if National Institute of Technology Karnataka (NITK) Surathkal serve upon us a written claim or demand on or before.....(date).  
This Bank further agrees that the claims if any, against this Bank Guarantee, shall be enforceable at our branch office at ..... situated at ..... (Address of local branch).

Yours truly,  
Signature and seal of the guarantor:  
Name of Bank & Address:  
Date:

**Instruction to Bank:** Bank should note that on expiry of Bond Period, the Original Bond will not be returned to the Bank. The bank is requested to take appropriate necessary action on or after expiry of bond period.

## BANK GUARANTEE FORMAT FOR EARNEST MONEY DEPOSIT / BID BOND

(To be typed on Non-judicial stamp paper of value Indian Rupees One Hundred)

(TO BE ESTABLISHED THROUGH ANY OF THE NATIONAL BANKS (WHETHER SITUATED AT MANGALORE OR OUTSTATION) WITH A CLAUSE TO ENFORCE THE SAME ON THEIR LOCAL BRANCH AT MANGALORE OR ANY SCHEDULED BANK (OTHER THAN NATIONALISED BANK) SITUATED AT MANGALORE. BONDS ISSUED BY CO-OPERATIVE BANKS ARE NOT ACCEPTED)

### LETTER OF GUARANTEE

To

Registrar,  
National Institute of Technology Karnataka,  
Srinivasnagar P.O., Surathkal  
Mangalore – 575025

IN ACCORDANCE WITH YOUR TENDER for the supply of ....., M/s. ....  
(hereinafter called the "Bidder") having its Registered Office at....., wish to participate in the said bid for the supply.....as an irrevocable Bank Guarantee against Earnest Money Deposit for an amount of Rs. .... (Rupees.....) valid up to **(180 days from the date of**

**issue of Bank Guarantee)**, is required to be submitted by the bidder as a condition precedent for participating in the said bid, which amount is liable to be forfeited by the Purchaser on (1) the withdrawal or revision of the offer by the bidder within the validity period, (2) Non acceptance of the Letter of Indent / Purchase order by the Bidder when issued within the validity period, (3) failure to execute the contract as per contractual terms and condition within the contractual delivery period and (4) on the happening of any contingencies mentioned in the bid documents.

#### **During the validity of this Bank Guarantee:**

We, .....(Bank name) having the registered Office at ..... guarantee and undertake to pay immediately on first demand by NITK Surathkal, an amount of Rs..... (Rupees. ) Without any reservation, protest, demur and recourse. Any such demand made by the NITK Surathkal shall be conclusive and recourse. Any such demand made by the purchaser shall be binding on the Bank irrespective of any dispute or difference raised by the Bidder.

The Guarantee shall be irrevocable and shall remain valid up to (180 days from the date of issue of Bank Guarantee) If any further extension is required, the same shall be extended to such required period on receiving instruction from the Bidder, on whose behalf the is Guarantee is issued.

#### **Notwithstanding anything contained herein:**

- \* Our liability under this Bank Guarantee shall not exceed Rs..... (Rupees.....).
- \* This Bank Guarantee shall be valid up to (date).
- \* We are liable to pay the guaranteed amount or any part thereof under this Bank Guarantee Only and only if you serve upon us a written claim or before (date).

This Bank further agrees that the claims if any, against this Bank Guarantee shall be enforceable at our branch office at ..... situated at .....(Address of local branch).

**Yours truly,**

Signature and seal of the guarantor:

Name of Bank:

Address:

Date:

**Instruction to Bank:** Bank should note that on expiry of Bond Period, the Original Bond will not be returned to the Bank. The bank is requested to take appropriate necessary action on or after expiry of bond period



**Detailed Technical Specifications**

**Item name: Altium PCB Design Software**

**Estimated Cost: Rs. 4.5 Lakhs**

**Number of licenses required:1**

1. **Altium PCB Design Software (Qty: 1) installed at Aditya Auto Products & Engineering (India) Private Limited, Bangalore.**

**AMC, Technical Support & Updates: One year.**

**Rate quoted should be inclusive of Testing, commissioning and Installation of Software and Training.**

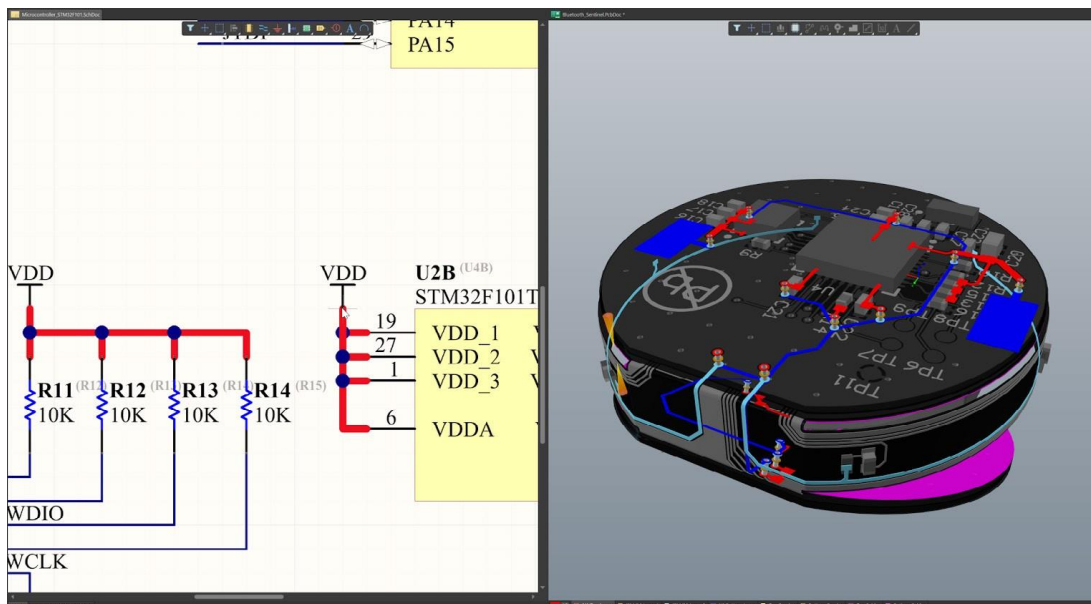
**Summary:**

The unified data model in Altium Designer enables rapid, efficient design of new electronic products with a synchronized, rules-driven approach. Streamlined uniformity of the user interface across all editors (Symbol, Footprint, Schematic, PCB, Documentation, etc.) makes the design process highly productive, removing traditional bottlenecks and errors caused by manual design synchronization across tools.

**Software capabilities:**

**Schematic Capture**

Every PCB design depends on accurate schematics. Whether you are starting from scratch or working on existing designs, schematic capture is fast and intuitive with our modern user interface. You can import designs from PCB design packages and get started on existing designs immediately. Altium Designer maintains a two-way connection between schematics and PCB to provide a unified interface throughout the design process, improving productivity and enabling cross-referencing between schematic and PCB layout.



Cross-Probe from schematic to PCB layout

### Design Import

Leverage previous designs reducing time re-creating schematics, board layouts, and associated design data with an automatic importer of project files from P-CAD®, EAGLE®, OrCAD®, PADS®, Xpedition® xDX Designer, Xpedition® Enterprise, CADSTAR®, and Allegro®.

You don't have to start from scratch facilitating switching, enabling learning about Altium Designer with a familiar project, and allowing switching during any stage of a project to Altium Designer.

### Unified Schematic and PCB layout

With cross probing and unified dataset, when you select an object on schematic that same object is selected on your PCB and vice versa. Cross probing automatically cross-references every net, pin, and component on the PCB to give the clearest insight into the implementation of schematics.

You can place related circuitry quickly and make better decisions on placement making it easier to get a successful layout on the first try. Plus, finding specific design aspects is easy with dedicated panels with all design details.

### Schematic Design Rules

You can add design rule "Directives" to the schematic - nets, wires, busses, harnesses, any component or sheet or document parameter. These are used to drive automated rules for correctly laying out the PCB to help get the board design right the first time.

Examples of this are differential pair definitions and length matching rules for DDR memory routing. Created design rules drive the routing and layout, saving time and also providing guidance from the schematic. You benefit by reducing the number of possible errors and helping identify existing errors, for example, collision errors with an enclosure. You will experience fewer errors and find them quicker reducing manufacturing and respin costs.

### Electrical Rule Checks

The Electrical Rule Checks (ERC) in schematic alert you to problems in the design. While Design Rule Checks (DRC) help layout the board correctly and meet manufacturing requirements, the Electrical Rule Check helps prevent you from making design mistakes at an engineering level.

For instance, connecting two output driving sources together will cause a rule violation and associated error message, so you prevent an electrical fault in the final, assembled circuit. You will experience fewer electrical errors and find them faster. ERC also reinforce the design will function correctly once manufactured.

### Hierarchical & Multi-channel Design

Electronic devices are generally complicated systems within systems. It's a natural desire to break up the design into pieces like blocks or modules, to "divide and conquer" the design. Also, it is often desirable to re-use specific circuit blocks in different designs, or as multiple channels within the same design. Altium Designer provides a Hierarchical Design

Environment enabling creation of designs at a block diagram top-level and allowing design projects to be split into manageable logical chunks (ie. Power Supply, Analog Front-End, Processor, IO, Sensors etc.) Hierarchical design also allows you to instantiate multiple copies of the same block when you need multiple channels of an identical circuit (e.g. audio-visual mixing equipment).

You save time on the PCB side by allowing the circuit layout and routing to be automatically duplicated for identical circuits. When a change is made, it can be made to the base logical chunk and the results will propagate through the design. Overall your work and potential rework is minimized and design integrity increases by reusing blocks.

### Design Designator Annotation

Annotation is a routine task that you have to perform to detail your work and maintain synchronization between different parts of your design. Annotation is the process of making critical or explanatory notes for the purpose of clarifying details. The most critical form of annotation is the systematic and methodical process for ensuring that each component is uniquely identified. Based on a component's designator, annotation is the primary means of referencing each component.

Annotation makes it possible to ensure that all the Schematic components remain related to their physical PCB implementation. PCB layout changes can result in a reassignment of designators or re-annotation, and these changes must be passed back to the Schematic environment.

Altium Designer automates how annotations are handled, tracked and verified, to keep design data in sync. Design integrity is boosted with synchronization between designators on the schematic and PCB level reducing errors.

### Component Management

Last-minute supply issues derail design timelines and increase costs. Component management leverages complete control over the component selection process to avoid any delays when manufacturing your board. Integrated supply chain information combined with specified alternate parts directly in the bill of materials (BOM) minimize the possibility of supply issues.

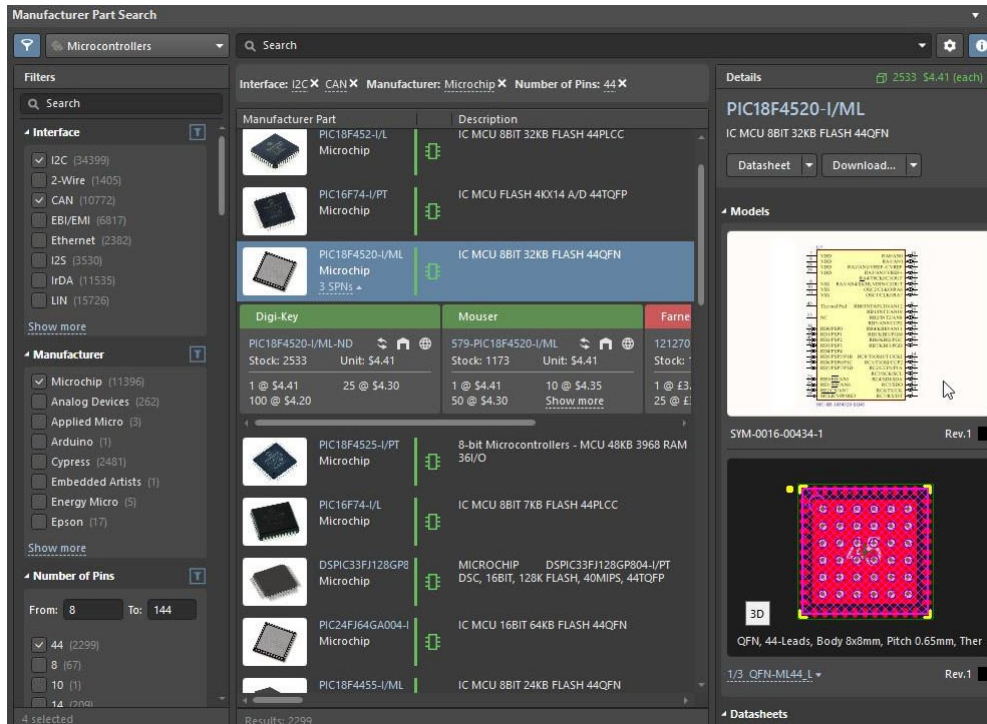
### Unified Component Model

Altium Designer uses different Library Types (Schematic, PCB, Database, etc) to define different aspects of a component (Symbol, Footprint, etc.) unified by a component library. Unified component models combine all defining information into a single, place able design part. Maintained libraries exist in the same ecosystem as the design environment allowing direct placement on a schematic and PCB layout level.

### Manufacturer Part Search and Components Placement

You can link parts with real-time pricing and availability data from personal parts suppliers and over 100 Altium verified suppliers. You can leverage price, availability, life-cycle status and real-time supplier information to meet their design goals. Utilizing the information reduces risks of last minute costs due to component supply chain issues. In turn, you can plan manufacturing reducing time to market and minimizing unexpected costs and design changes.

With the Manufacturer Part Search, rapidly find which parts are available and at what costs - right at design time. And why waste time making the parts every time? If symbol and footprint models are available in the Altium content ecosystem, you can either acquire them from the parts search panel to your own library for customization, or simply place them directly in your design.



Streamlined part search

Placing parts into your design from anywhere - libraries, data management servers, or the cloud, is a snap. Through a single unified Components panel, all the parts and rapid parametric search and filtering will let you find exactly the part you need, right when you need to place it.

From Altium Designer 19 on, you can connect your engineering desktop to Altium's new cloud based collaboration and data management solution, Altium 365, to keep components organized, gather usage statistics, and update components to the latest revision with the click of a button.

### Real-Time BOM Management

The Bill of Materials (BOM) is a list with the necessary parts used in a design for manufacturing.

ActiveBOM provides you with automation by supplying part information such as availability and price from selected suppliers.

Altium Designer allows specifying pin-compatible backup part choices directly in the Bill of Materials (BOM) referred to as Alternative Part Choice. Having pin-compatible backup part choices nearly eliminates supply chain issue risks for manufacturing. In turn, you can design taking into account potential manufacturing blowouts reducing time to market and minimizing unexpected costs and design changes.

### IPC Compliant Footprint Wizards

No need to spend hours copying and pasting pads on BGAs or rummaging for component 3D models. And no need to pay for expensive 3rd party software wizards for building IPC- 7351 compliant footprints. All that is built-in to Altium Designer, and with each release new footprint types and updates are added. Any part you need can be rapidly and accurately built to match your own library standards while also meeting the fabrication and assembly quality and layout set forth by IPC-7351, SM-782 and JEDEC (through hole). You can even batch produce whole families of footprints from an Excel sheet or CSV file.

### Mixed Simulation

Altium Designer allows you to easily create and manage multiple simulation profiles. Separate profiles allow designers to run different types of analyses with different simulation engines (Mixed Sim, SIMetrix, SIMPLIS). This allows multiple runs of the same simulation type (e.g., AC analysis) with different parameters and options (e.g., different frequency ranges). Active profiles can easily add, remove, edit, run, and/or generate netlists. The Profile Manager organizes profiles and uses probes or active nets to select waveforms to display. All simulation results can be saved with other manufacturing outputs for conveyance to manufacturing. You can convey design intent to the contact manufacturer minimizing errors.

### Board Layout

The screenshot shows the Layer Stack Manager interface. On the left is a table of board layers, and on the right is a detailed view of the selected impedance profile and transmission line parameters.

Top Ref	Bottom Ref	Width	Etch	Gap	Z	Z Dev...	Tp
2 - SPLIT2		0.086mm	Inf	0.127mm	93.015...	0.016%	5.5294...
1 TOP	3 - S3	0.051mm	Inf	0.127mm	93.011...	0.012%	6.836n...
2 - SPLIT2	4 - VDD4	0.083mm	Inf	0.127mm	92.973...	0.029%	6.836n...
3 - S3	5 - S5	0.083mm	Inf	0.127mm	92.973...	0.029%	6.836n...
4 - VDD4	6 - S6	0.083mm	Inf	0.127mm	92.973...	0.029%	6.836n...
5 - S5	7 - SPLIT7	0.083mm	Inf	0.127mm	92.973...	0.029%	6.836n...
6 - S6	8 - BOTTOM	0.051mm	Inf	0.127mm	93.011...	0.012%	6.836n...
7 - SPLIT7		0.086mm	Inf	0.127mm	93.015...	0.016%	5.5294...

**Layer Stack Manager**

Search

**Impedance Profile**

Description: 2

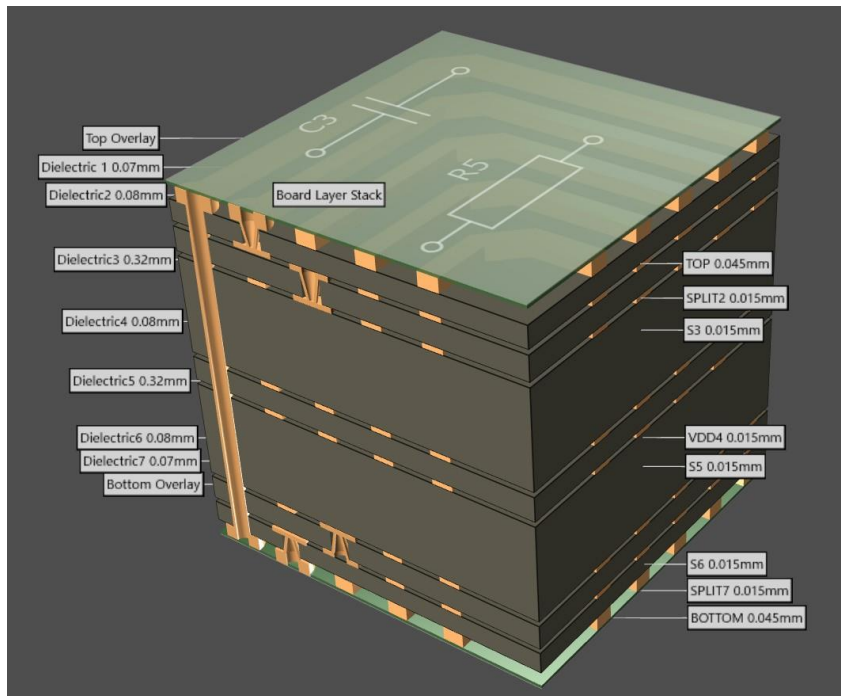
Type: Differential

Target Impedance: 93Ω

Target Tolerance: 10%

**Transmission Line**

$H1 = 0.07\text{mm}$   
 $Er1 = 4.2$   
 $H2 = 0.08\text{mm}$   
 $Er2 = 4.2$   
 $T = 0.015\text{mm}$   
 $W1 = 0.051\text{mm}$   
 $W2 = 0.051\text{mm}$   
 $S = 0.127\text{mm}$





## Layer Stack Manager

Design the most organized and efficient board layout with the ability to place and drag components that push, avoid, and snap-to alignment with other objects and pads on your board layout. These features make laying out dense boards much easier, and maintain design rule compliance as well. Signal integrity disturbances are reduced on high-speed PCBs with complete control over every drill hole with hole tolerances and back drilling capabilities.

## Visual Layer Stack Management

Layer stack management allows you to define the material composition and specialized regions on the board. For flex circuitry, rigid-flex and embedded technology PCB designs, you can control the entire stackup, including all rigid and flex portions with bending angles and individual layer definitions. You can visualize layer stacks using subsets of materials used in the primary layer stack. Each layer has an individual definition and corresponding parametric data from the Materials Library.

Complex boards with multiple stackups can be defined side by side to facilitate board construction. You define and manage all of the layer stackups in a central location to facilitate tracking of layer stack details and minimizing errors and miscommunication on layer details.

## Materials Library

The Materials Library contains system-wide parametric data on any materials you may specify in the construction of your layer stack. From dielectric cores and prepregs with different base thicknesses and glass weaves, to electro-deposited and rolled coppers, to glue pastes, conductive inks, and films - it's all there. And you can create any new materials you intend to use, or use the set of generic ones already there, and the materials library can be saved and loaded to XML - so you can share it with the entire team.

## Fearless HDI™

Fearless HDI (High Density Interconnect) is our technology for enabling accurate design and visualization of HDI structures, including laser-drilled and mechanical microvias, stacked microvias, skip-vias.

A dedicated Layer Stack Manager tab allows you to define what  $\mu$ Via, blind/buried and other via structures you can allow in your project, and control the layer stack symmetry.

During routing of the board, the HDI via structures can be chosen interactively or used for fanning out parts on surface layers. Changing layers can automatically stack them as defined in the layer stack manager.

## Impedance Profiles

More and more modern designs require accurate control of trace impedances (single and differential pair) to maintain signal integrity. USB 3.0, Type C, DDR4/5 and RF/ $\mu$ wave designs all require accurate planning of the trace widths, gaps, and layer stack in order to maintain correct transmission line impedances across the board.

Impedance profiles in the Layer Stack Manager use a fast, accurate 2D field solver to calculate impedances from trace widths, and trace widths and spacings from impedance. Single-ended and differential microstrip or striplines including asymmetric planes can be specified using plane layers or signal layers for references.

Impedance profiles are then used in design rules to automate the correct trace or pair characteristics during interactive routing, or to test for impedance within the desired tolerances. The hardware designer can drive it either way for accurate results.

## Panelization

Panelization is the process of placing several designs on a single board for manufacturing. The boards break apart and can be used separately. The process is generally used for smaller, less complex designs and the panel can contain the same design or various small designs.

### Rules Driven Design

You can easily define design rules and rule prioritization hierarchy. Design rules compliance as You progress keep the layout manufacturable and enable design intent communication to manufacturing based on part parameters. Design rules check for issues as you is designing, preventing issues before they stack up. Specific manufacturing guidelines with a customizable design rule system include specifications for board outlines, solder mask expansions, drill placement, and an advanced query editor to create non-standard rules.

With design rules, You can complete right-first-time designs. Created design rules drive the routing and layout, saving time and also providing guidance for the PCB designer. You benefit by reducing the number of possible errors and helping identify existing errors, for example, collision errors with an enclosure. You will experience fewer errors and find them quicker leading to a reduction in time to market, reducing manufacturing and respin costs, and increase in design integrity.

### Copper Pour Management

Copper regions are used to make connection in a PCB. They are commonly used to create power plane and signal planes to connect to components and can be used to help with heat distribution. Stand-off regions are required distance from one copper region to another to prevent interference between the connections. PCB designers generally use filled copper regions to cover the remaining area outside those tracks, pads, and stand-off regions. You can control the placement (pour) order and temporarily disable (shelve) regions to make it easier to see underlying PCB layout.

In Altium Designer areas of copper can be defined using three different design objects: Fills, Solid Regions and Polygon Pours. The advantage of a Polygon Pour is that it automatically creates stand-off regions to copper objects that belong to another net based on Design Rules. The automation of copper region placement increases design integrity and productivity and minimizes design errors.

### Precise Object Placement

There are always board areas that require special considerations and rules to maintain a viable design. Altium Designer incorporates the use of rooms, keep outs, and polygon regions to aid you when designing. Rooms are regions that assist in the placement of components by grouping them inside the designated area. On the other hand, keep out regions act as an 'interference' object that prevent other copper objects from intersecting its area, as specified by the global clearance rule. Lastly, polygons act as regions in the board to dictate allowable copper pour areas, as well as defining copper pour order.

Precise placement defines the PCB layout to facilitate routing and avoid physical collisions. You can minimize errors, complete designs faster, and get the product to market faster. The added benefit of precise fit to minimize risk of respin and maximize first pass manufacturing.

### Advanced Snap Points and Grids

Grids define spacing for the entire board. Snap points are defined locations in 3D space that make it easy to align 3D bodies (ie enclosure to board or mounting holes). Combining customisable grids, definable snap points, and 3D body/Pad alignment, every aspect of a user's design is placed with complete precision.

Precise placement defines the PCB layout to facilitate routing and avoid physical collisions. You can minimize errors, complete designs faster, and get the product to market faster. The added benefit of precise fit to minimize risk of respin and maximize first pass manufacturing.

### Rigid-Flex and Multi-Board

Altium Designer makes it simple to define and modify the shape of a board.

NATIVE3D™ gives a realistic view of what a manufactured board will look like when produced. This lets you view, rotate, and translate your design so that you can visually check all clearances.

Layer Stack Regions allow a single board to be composed of multiple materials, flexibility, and thickness, enabling design of Rigid-Flex-Rigid PCB assemblies.

### Rigid-flex regions with bend angles

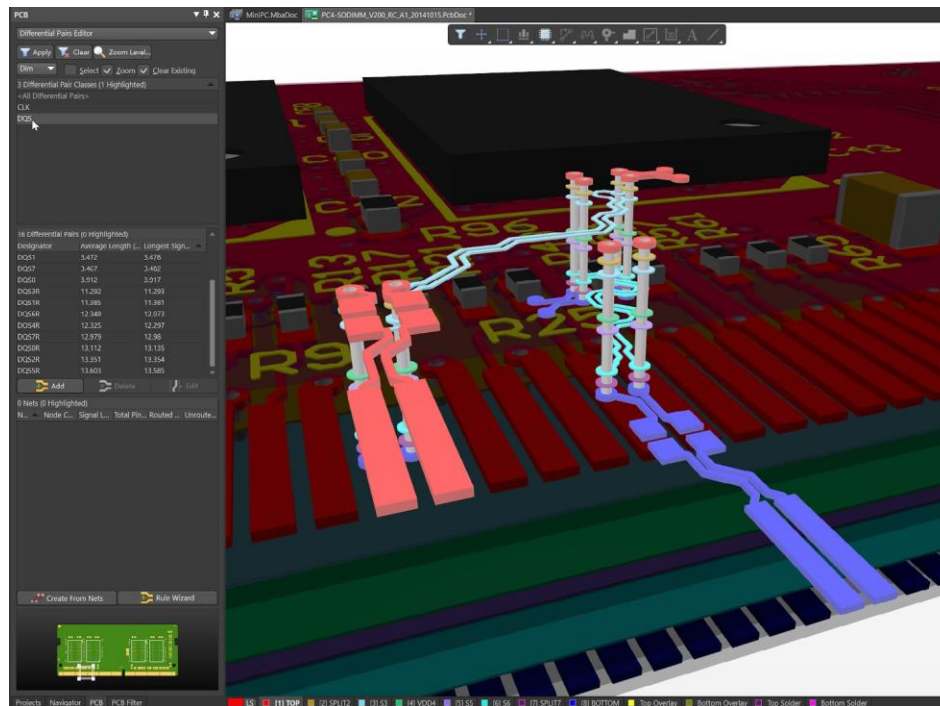
You can add rigid-flex sections to the PCB design with bikini coverlay support and check clearances with NATIVE 3D. All board movement is controlled with definable angle, radius, and fold index for rigid-flex regions. One of the most valuable features lets you create full-motion video clips from board 3D snapshots to convey design intent to manufacturing.

This is critical in designs that use multiple folds to fit in tight spaces or allow movement of the flex circuitry. You can gain confidence in flex and rigid-flex PCBs by confirming board fits in a mechanical enclosure without the financial and time cost of a physical prototype. Reduced prototyping costs resulting in reduced time to market and manufacturing/repin costs.

### Interconnected Multi-board Assembly

Multi-board design means design of unitary electronic systems that have multiple boards or modules housed together and electrically interconnected in some way sometimes referred to as modular design.

Modular design effectively means developing each board in the multi-board system as a complete functional unit. Each module forms a distinctly reusable object (logical and physical) within the broader system. A good example of this would be the DDR4 SDRAM memory modules within a server or desktop PC.



PCB design using NATIVE 3D Technology

You gain efficiency and have fewer design errors when developing multi-board PCB based electronic systems in Altium Designer. Automation helps define the way boards will interconnect and the signals that go between them. Reduced errors, time to market, and costs and increase in design integrity.

### MCAD Collaboration

Collaboration is essential for a successful design process. Altium Designer connects your PCB design workflow to the complete engineering ecosystem with powerful MCAD collaboration features and fully managed library management systems. Finding out your board interferes with a connector at the prototype phase is a costly error. Ensure your board fits the mechanical enclosure right the first time with NATIVE 3D clearance checking.

### Perfect fit mechanical enclosures



The main offering to ensure fit, NATIVE 3D capabilities, allow clear 3D modelling with real time clearance checking. ECAD/Mechanical CAD collaboration is simple because we can use popular mechanical models directly in the design environment.

You import 3D models and mechanical enclosures from MCAD systems to have the most realistic, accurate, and data-rich 3D models for an exact representation of a physical board without the need for costly prototypes. The IPC-compliant PCB Component Wizard handles any other 3D model needs with a guided process for custom component creation. You get reduced prototyping costs resulting in reduced time to market and manufacturing/repin costs.

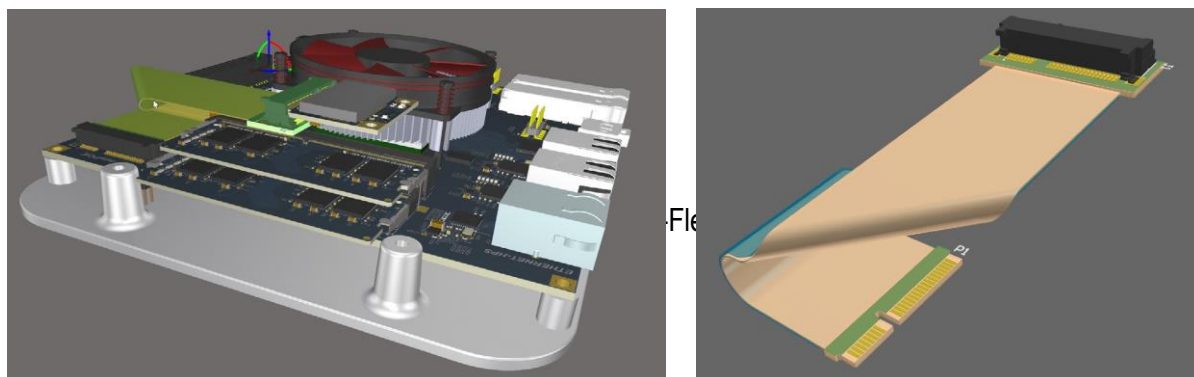
#### Mechanical Model Import

Altium Designer Libraries, PCB Documents, and Multiboard Assemblies all support import and creation of 3D solid models using STEP. Parasolid is also supported with the optional MCAD Collaboration Plugin.

Even the 3D PCB shape can be imported from a mechanical CAD (MCAD) model, via STEP, DXF/DWG, IDF and IDX Baselines. IDF and IDX are not only used for modifying the board shape, but can relocate and re-orientate moved components, allowing bi-directional synchronization between mechanical and PCB layout.

MCAD import into Altium Designer provides more than just a slick visualization of your PCB before you've made it. It allows the PCB design rules engine to immediately inform you of component body collisions and clearance violations in the 3D space of the assembly.

MCAD import of enclosure models allows the PCB designer to use key features of the 3D enclosure and other mechanical objects for alignment and for creation of the board shape from a projected surface.



Multi-Board and Rigid-Flex Design

#### Interactive Routing

You can design the highest quality PCB layouts in a fraction of the time with an advanced routing engine that includes push and shove, hug, walk around, and interactive length tuning modes for single and differential pair routes. Fully configurable single and differential pair routing in Altium Designer also provides phase and delay tuning across terminations and complex topologies using xSignals™. ActiveRoute® lets you control where and how much automated routing assistance you want on a net connection level up to your whole design. Visual clearance boundaries between traces and components on your board let you visualize design rules and understand your layout at a glance.

#### Single and Multiple Length Tuned Traces

The interactive routing modes in Altium Designer help You lay out boards quickly with precise control over the organization and flow of your board layout. They can interactively route their board with several powerful routing options including autoroute, walk around, push, hug and push, ignore obstacle, push & shove, and differential pairs. They can even automatically align routing path lengths without ever having to waste time manually adjusting individual nets with interactive length tuning.

You can leverage routing automation to route their designs quickly and accurately reducing the repetition of the task. You can spend more time perfecting their design leveraging the speed enhancement and implemented design rules of the interactive routing. Combined with design rules and design objects (rooms, keepouts, etc) you can reduce errors, achieve first pass manufacturing, and get to market faster.

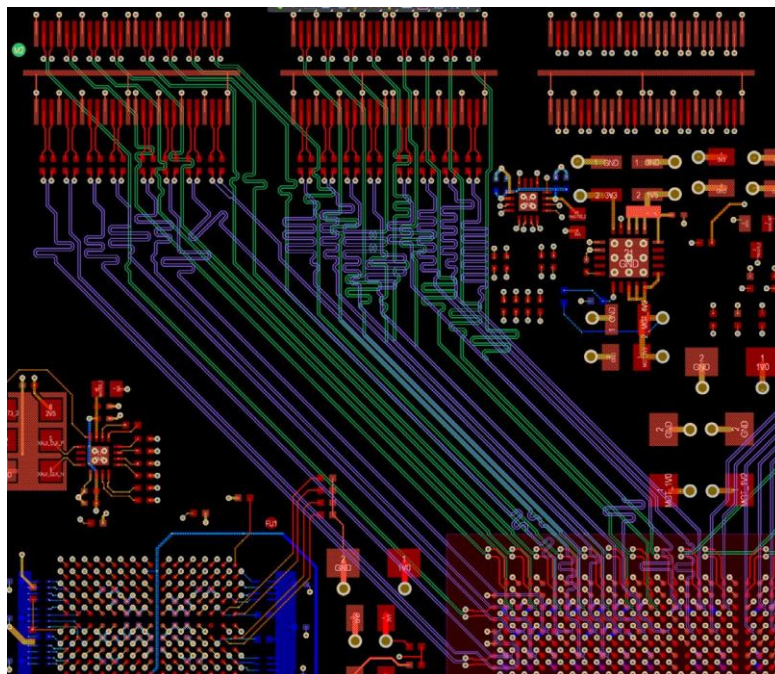
### Automated High-Speed Signals for High Speed Topologies

Working with high-speed designs can be time-consuming. The xSignals wizard lets you easily plan and constrain your high-speed designs by defining high-speed signal paths for modern technologies. They can route high-speed designs with fully configurable differential pair routings that carry precise signal lengths across their PCB. DDR3/4 and USB3.0 signals are automatically identified by the wizard creating rules to keep all signals in sync and tuned to the correct length.

You can minimize timing errors for their signals. The signals are grouped together to ensuring organization and traceability while facilitating error correction and precise length tuning. The risk for design respins is minimized and the product design can go to market faster.

### Fast and High-Quality Routing

ActiveRoute is a tool that lets you select where and how much automation you want to employ along selected nets. The technology in ActiveRoute coupled with user guidance produces high-quality layouts in seconds. ActiveRoute lets you breakout and route large, fine-pitch BGAs by instructing it where to route them (ie select layers, draw a guide), and letting it route for you. Unlike other interactive routing technologies, ActiveRoute works on multiple layers simultaneously while using all design rules. By routing on multiple layers simultaneously, routing is faster, traces can be evenly distributed, and the ability to complete the routes increases significantly. Errors are minimized, time to market is reduced, and first pass manufacturability is promoted.

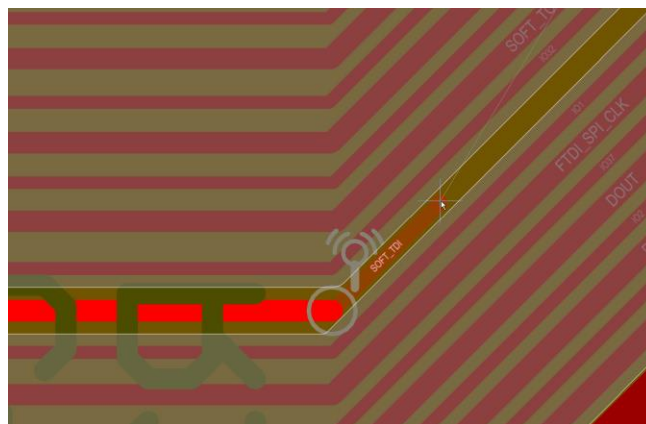


ActiveRoute with Guided Path and Tuning for High Speed Design

By routing on multiple layers simultaneously, routing is faster, traces can be evenly distributed, and the ability to complete the routes increases significantly. Errors are minimized, time to market is reduced, and first pass manufacturability is promoted.

### Visual Clearance Boundaries

You can visually see clearance boundaries between traces and components during route placement. Understanding the impact of your routing decisions in real-time alleviates the stress from unclear obstacles in the design process. You can route through high-density areas with certainty that traces fit where they need them. You have immediate feedback to how route placement changes their layout and how it will change future routes. Errors are minimized, time to market is reduced, and first pass manufacturability is promoted.



Running a trace through a congested area

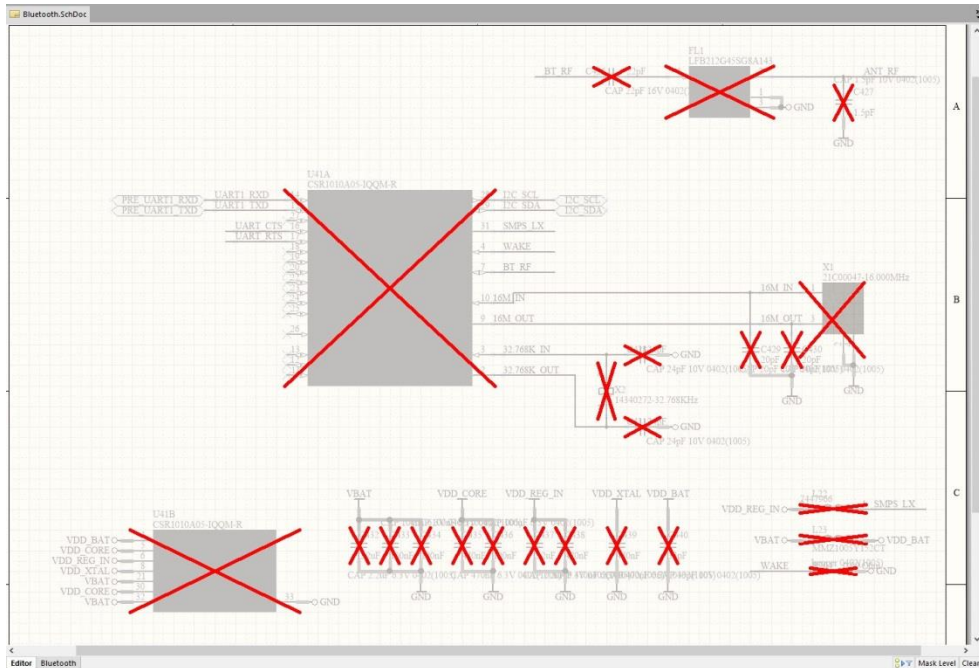
### Manufacturing Documentation

When you are ready to move finished design into manufacturing, clear communication is mandatory. Output jobs act as an organized, reusable container for all necessary design outputs. Clear design intent communication to manufacturing is simple with powerful release management and automated documentation tools built into Altium Designer.

#### Automated Documentation Outputs and Project Release

Altium Designer enables you to add verified project snapshots into your workspace, or desired folder structure with the streamlined project releaser. You can dynamically create customized project outputs for design variants linking fabrication and assembly outputs with the latest design source files.

With an organized release process, output generation gains consistency and accuracy while ensuring You don't use out-of-date design files. The result is conveyance of design intent to the contract manufacturer of the completed design. Reduced time to market, first pass manufacturability, and increased design integrity.



This example shows a variant of a design with Bluetooth circuitry omitted

### Visual Manufacturing Outputs

Altium Designer's CAM Editor (CAMtastic!®) offers a variety of tools, the most basic of which are for viewing and editing CAM data. Once image and drill files have been imported, the CAM editor can extract physical connectivity netlist and compare it with an IPC netlist generated from the original PCB design software. These netlists will handle not just through-hole components, but blind and buried vias as well. The CAM Editor also offers Design for manufacturing Rule Checking, copper thieving, panelization and NC-Routing (plus milling) tools.

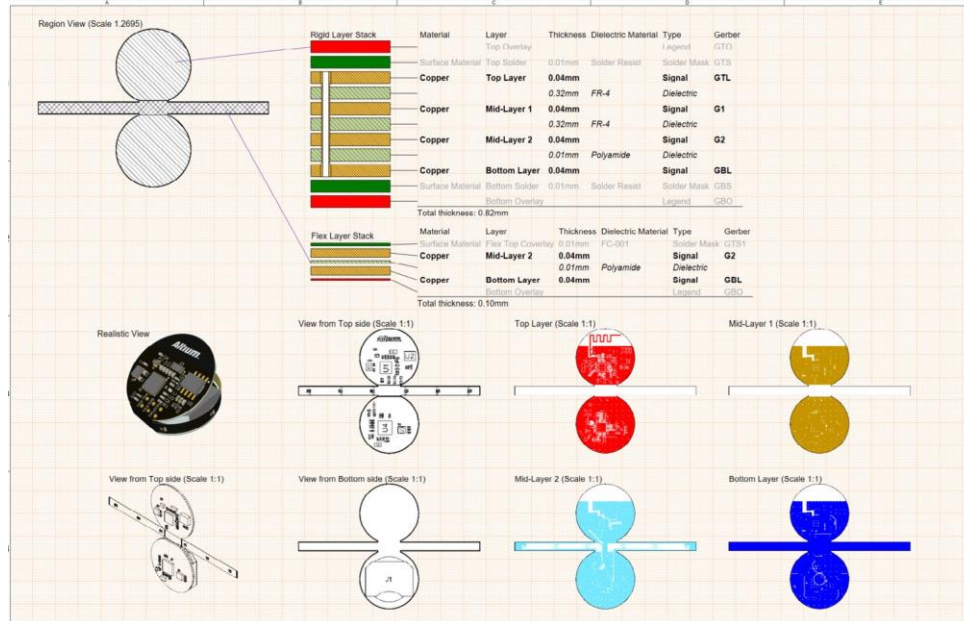
You can view the manufacturing outputs of their design to gain insight to what the contract manufacturer will receive. This insight allows you to make changes at identified problem areas. It also allows you rudimentary reverse engineering capabilities to create a skeleton PCB from manufacturing files. Increased design integrity, design intent communication, and first pass manufacturability.

### Unified Professional Documentation Process

You can create assembly and fabrication documentation directly linked to source designs with Draftsman® and update their entire documentation at the click of a button. They can create templates for documentation that only require minimal customization across designs. They can add PCB dimensions, measurements, notes, and callouts between points of interest (datums) and design objects to customize documentation workflow.



The set of powerful and easy-to-use features integrated in Altium Designer automate documentation ensuring consistency. You benefit from guaranteed updates to documentation and a unified workflow. The possibility for data mismatch is practically eliminated, and there's no need to export your design to DXF/DWG or other file formats into archaic 2D drawing tools. Reduced time to market, increased design integrity, design intent communication, and first pass manufacturability are the result.



Fabrication Documentation generated in Draftsman.

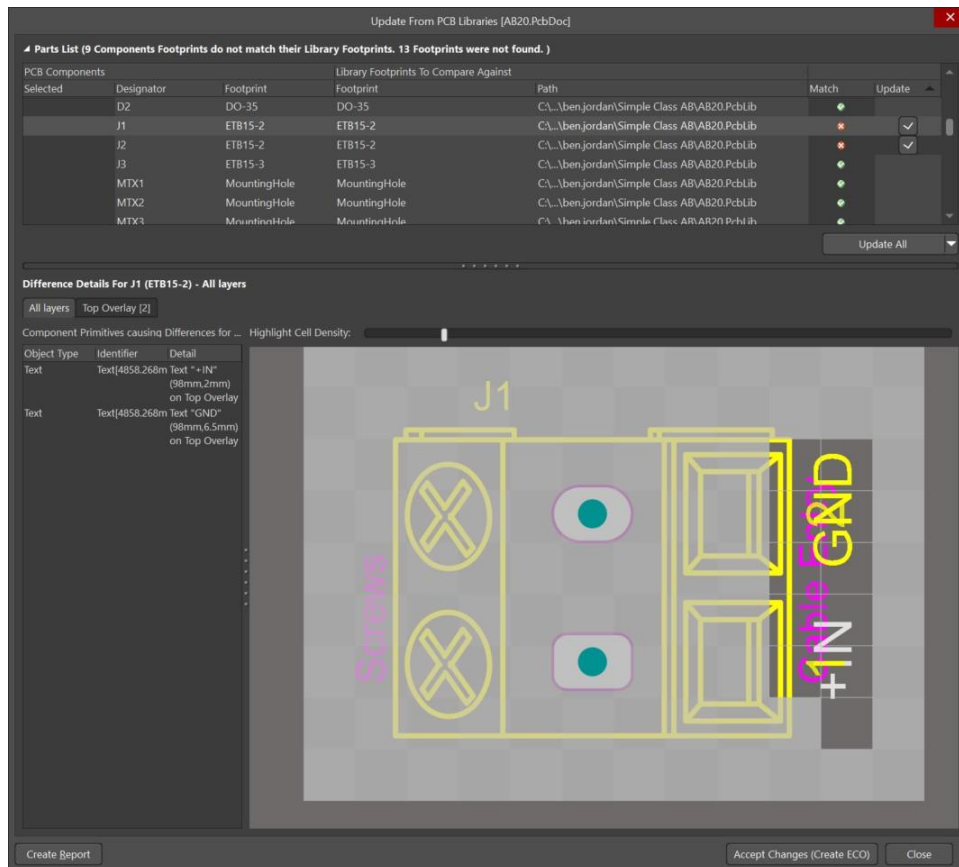
### Data Management

Keeping track of design data is a complicated process with differing opinions of what is "correct." It is important to synchronize methods across a team to facilitate compliance, reduce the strain of maintenance, and ensure consistency across designs. Altium Designer leverages common software design techniques of version control and reusable design materials to synchronize design teams and allow you to get started on the right path.

### Version Control

Version control allows you to save and maintain file revisions in an organized structure. Altium Designer integrates two important version control systems: GIT and subversion version control (SVN) support. Version control makes it possible to use design tracking, change permissions, and track collaboration. Designers can check-in, check-out, and visually compare differences between revisions of components, schematic documents, and PCB projects.

Version control helps with collaboration on projects and makes it easy to visually track changes across file revisions reducing time for error recognition and resolution reduces time to market and increase design integrity.



Version comparison of component.

## Design Reuse

Templates create a uniform design unit to keep design information organized. The design units range from as small as pads to full project types to act as a common baseline for all new design materials.

Snippets are saved pieces of circuitry on a schematic and PCB level that can be used on any design to leverage common circuitry.

Device sheets allow you to create known circuitry blocks for reuse across designs. They differ from snippets by increased complexity and predefined interconnection to other parts of the design. For example, a power supply system that has a defined output of 5 Volts to power another circuit on the design.

You save time on the Schematic and PCB side by allowing the circuit layout and routing to be reused. When a change is made, it can be made to the base logical chunk and the results will propagate through the design. Overall, you minimize work and potential rework and increase design integrity by reusing blocks reducing time to market and minimizing errors.

## Release Management

Whether you're using a formal managed process or working standalone, release management in Altium Designer helps hardware developers generate a complete package for going to prototype and production, lacking nothing.

What's more, the release process is completely repeatable, letting you create templates and preset output jobs that guarantee the same formatting and collection of design CAM (Fabrication), Documentation, Validation, and Assembly outputs, every time.

The Project Releaser works with your predefined manufacturing outputs, combined with electrical and design rule checking and BOM generation, to achieve consistent results while allowing you to archive any production design

snapshot in time, so you can always get back to the production restore point and compare changes. Release Management in Altium Designer gives you confidence.

#### Board Variants

You can create multiple versions of a board design with modifications to objects and other design elements to create unique products from the same base design (think iPod or phone variants with bigger hard drives, but some base design). Each variant stands as an original design with different components, version-specific design elements, and unique outputs to send to manufacturing.

You save time in duplicating a design for a variant creation while ensuring changes to the base design will not need to be duplicated. Sharing the same base design allows you to create multiple products with the same set of files and all documentation can be produced at the same time. You benefit with increased consistency, organization, and traceability minimizing time to market and potential respin and redesign costs.

**Timeline Requirement:** The system should be delivered to M/s Aditya Auto, Pvt Ltd, Bangalore within 04 weeks of Purchase Order release.

Delivery Address: **M/s Aditya Auto Products and Eng (I) Pvt Ltd**  
180, Bommasandra Industrial Area  
Bengaluru – 560099